

# DATA SHEET

## **74LV107**

Dual JK flip-flop with reset;  
negative-edge trigger

Product specification  
Supersedes data of 1997 Feb 03  
IC24 Data Handbook

1998 Apr 20

## Dual JK flip-flop with reset; negative-edge trigger

74LV107

## FEATURES

- Wide operating: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Output capability: standard
- $I_{CC}$  category: flip-flops

## DESCRIPTION

The 74LV107 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT107.

The 74LV107 is a dual negative-edge triggered JK-type flip-flop featuring individual J, K, clock ( $\overline{nCP}$ ) and reset ( $\overline{nR}$ ) inputs; also complementary Q and  $\overline{Q}$  outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ( $\overline{nR}$ ) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the  $\overline{Q}$  output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay nCP to nQ nCP to nQ nR to nQ, nQ	$C_L = 15$ pF; $V_{CC} = 3.3$ V	15 15 15	ns
$f_{max}$	Maximum clock frequency		77	MHz
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per flip-flop	$V_I = \text{GND to } V_{CC}^1$	30	pF

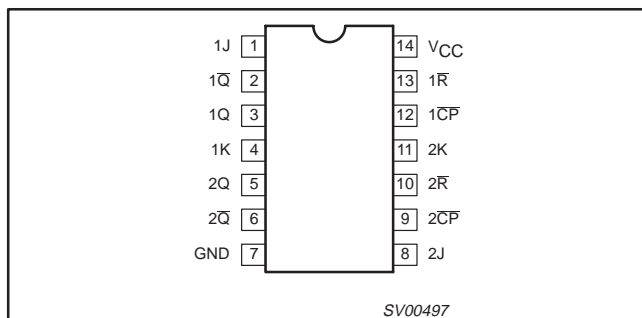
## NOTE:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV107 N	74LV107 N	SOT27-1
14-Pin Plastic SO	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV107 D	74LV107 D	SOT108-1
14-Pin Plastic SSOP Type II	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV107 DB	74LV107 DB	SOT337-1
14-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV107 PW	74LV107PW DH	SOT402-1

## PIN CONFIGURATION



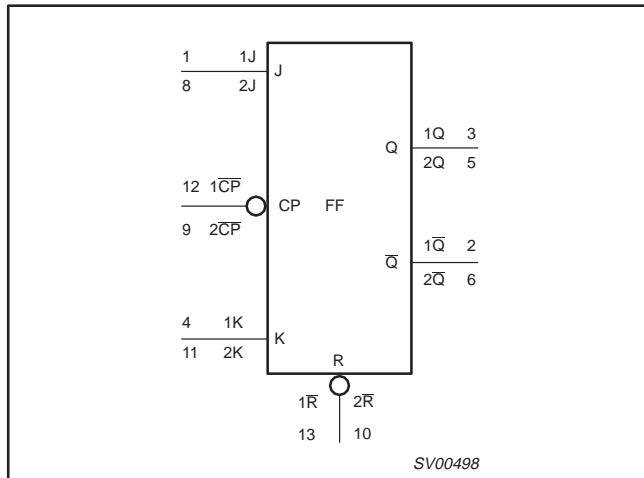
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	Synchronous inputs; flip-flops 1 and 2
2, 6	$1\overline{Q}$ , $2\overline{Q}$	Complement flip-flop outputs
3, 5	1Q, 2Q	True flip-flop outputs
7	GND	Ground (0 V)
12, 9	$1\overline{CP}$ , $2\overline{CP}$	Clock input (HIGH-to-LOW, edge-triggered)
13, 10	$1\overline{R}$ , $2\overline{R}$	Asynchronous reset inputs (active LOW)
14	$V_{CC}$	Positive supply voltage

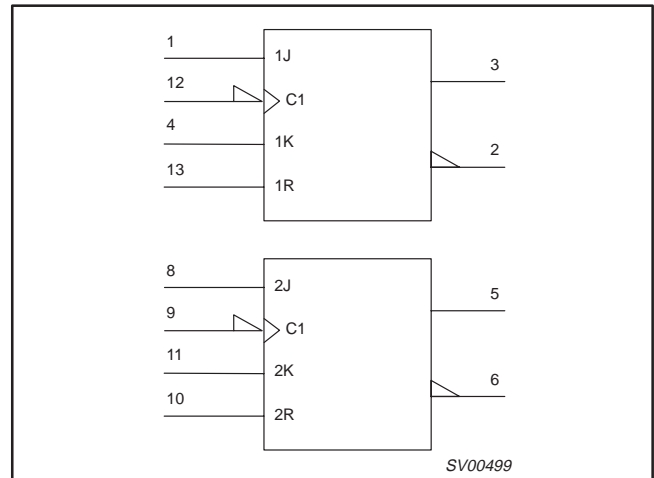
# Dual JK flip-flop with reset; negative-edge trigger

74LV107

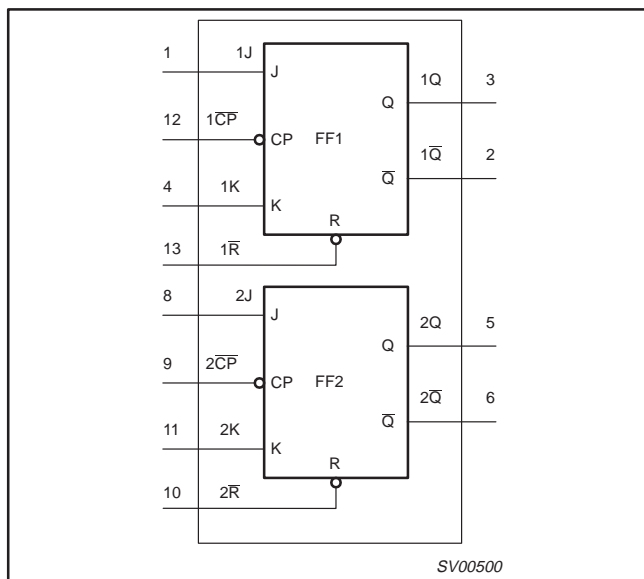
## LOGIC SYMBOL



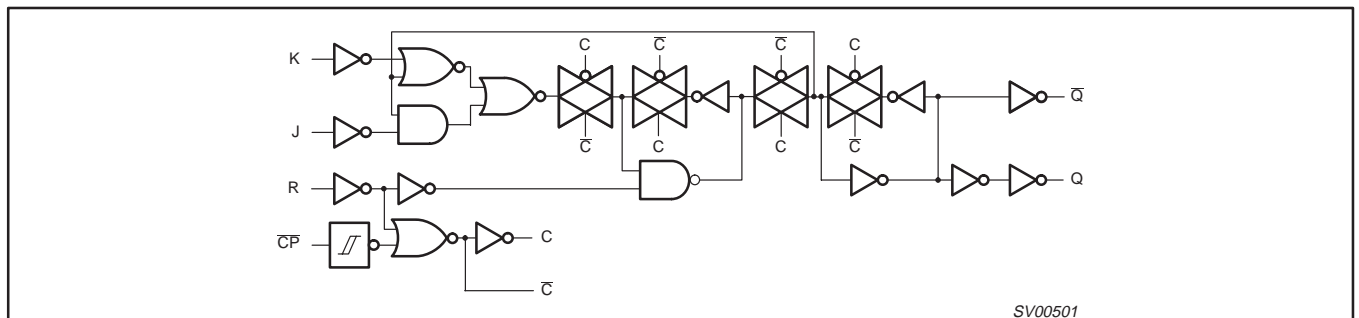
## LOGIC SYMBOL (IEEE/IEC)



## FUNCTIONAL DIAGRAM



## LOGIC DIAGRAM



## Dual JK flip-flop with reset; negative-edge trigger

74LV107

## FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	nR	nCP	nJ	nK	nQ	nQ
Asynchronous reset	L	X	X	X	L	H
Toggle	H	↓	h	h	$\bar{q}$	q
Load "0" (reset)	H	↓	l	h	L	H
Load "1" (set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\bar{q}$

## NOTES:

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition.

X = don't care

↓ = HIGH-to-LOW CP transition

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – standard outputs		50	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1	1.0	3.3	5.5	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
$t_r, t_f$	Input rise and fall times except for Schmitt-trigger inputs	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

## NOTE:

- The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 5.5V$ .

## Dual JK flip-flop with reset; negative-edge trigger

74LV107

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2 V	0.9			0.9		V
		V <sub>CC</sub> = 2.0 V	1.4			1.4		
		V <sub>CC</sub> = 2.7 to 3.6 V	2.0			2.0		
		V <sub>CC</sub> = 4.5 to 5.5 V	0.7 * V <sub>CC</sub>			0.7 * V <sub>CC</sub>		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2 V			0.3		0.3	V
		V <sub>CC</sub> = 2.0 V			0.6		0.6	
		V <sub>CC</sub> = 2.7 to 3.6 V			0.8		0.8	
		V <sub>CC</sub> = 4.5 to 5.5			0.3 * V <sub>CC</sub>		0.3 * V <sub>CC</sub>	
V <sub>OH</sub>	HIGH level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA		1.2				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	1.8	2.0		1.8		
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.5	2.7		2.5		
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.8	3.0		2.8		
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	4.3	4.5		4.3		
V <sub>OH</sub>	HIGH level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 6mA	2.40	2.82		2.20		V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 12mA	3.60	4.20		3.50		
V <sub>OL</sub>	LOW level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
V <sub>OL</sub>	LOW level output voltage; STANDARD outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.25	0.40		0.50	V
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.35	0.55		0.65	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND			1.0		1.0	µA
I <sub>CC</sub>	Quiescent supply current; flip-flops	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			20.0		80	µA
ΔI <sub>CC</sub>	Additional quiescent supply current per input	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V			500		850	µA

**NOTE:**1. All typical values are measured at T<sub>amb</sub> = 25°C.**AC CHARACTERISTICS**GND = 0V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nCP to nQ, nQ	Figures 1, 2	V <sub>CC</sub> (V)						ns
			1.2		95				
			2.0		32	44		56	
			2.7		24	33		41	
			3.0 to 3.6		18 <sup>2</sup>	26		33	
4.5 to 5.5			22		28				

## Dual JK flip-flop with reset; negative-edge trigger

74LV107

**AC CHARACTERISTICS (Continued)**GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 1\text{K}\Omega$ 

SYMBOL	PARAMETER	WAVEFORM	CONDITION	-40 to +85 °C			-40 to +125 °C		UNIT
			$V_{CC}(\text{V})$	MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$t_{\text{PHL}}/t_{\text{PLH}}$	Propagation delay nR to nQ, nQ	Figures 1, 2	1.2		95				ns
			2.0		32	44		56	
			2.7		24	33		41	
			3.0 to 3.6		18 <sup>2</sup>	26		33	
			4.5 to 5.5			22		28	
$t_w$	Clock pulse width HIGH or LOW	Figure 2	2.0	34	14		41		ns
			2.7	25	10		30		
			3.0 to 3.6	20	8 <sup>2</sup>		24		
			4.5 to 5.5	15			18		
$t_w$	Reset pulse width LOW	Figure 2	2.0	34	14		41		ns
			2.7	25	10		30		
			3.0 to 3.6	20	8 <sup>2</sup>		24		
			4.5 to 5.5	15					
$t_{\text{rem}}$	Removal time nR to nCP	Figure 2	1.2		35				ns
			2.0	24	12		29		
			2.7	18	9		21		
			3.0 to 3.6	14	7 <sup>2</sup>		17		
			4.5 to 5.5	11			14		
$t_{\text{su}}$	Set-up time nJ, nK to CP	Figure 1	1.2		40				ns
			2.0	26	14		31		
			2.7	19	10		23		
			3.0 to 3.6	15	8 <sup>2</sup>		18		
			4.5 to 5.5	12			15		
$t_h$	Hold time nJ, nK to CP	Figure 1	1.2		-10				ns
			2.0	5	-3		5		
			2.7	5	-2		5		
			3.0 to 3.6	5	-2 <sup>2</sup>		5		
			4.5 to 5.5	5			5		
$f_{\text{max}}$	Maximum clock pulse frequency	Figure 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70 <sup>2</sup>		20		
			4.5 to 5.5	30			24		

**NOTES:**

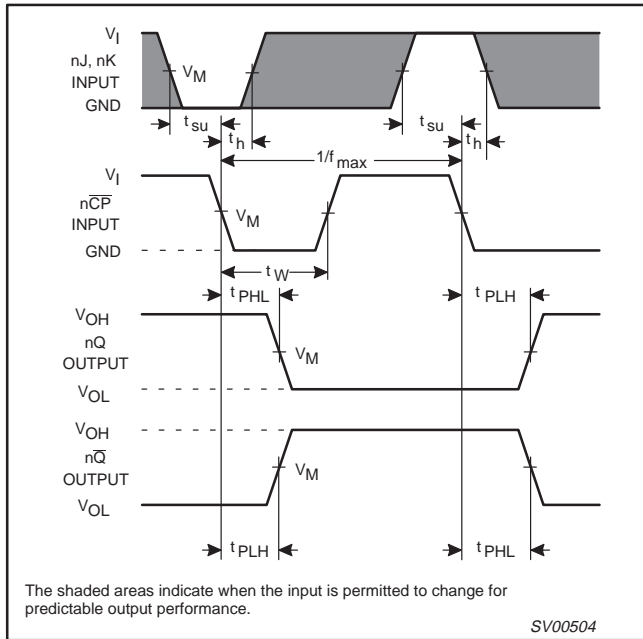
1. Unless otherwise stated, all typical values are measured at  $T_{\text{amb}} = 25^\circ\text{C}$
2. Typical values are measured at  $V_{CC} = 3.3\text{V}$ .

# Dual JK flip-flop with reset; negative-edge trigger

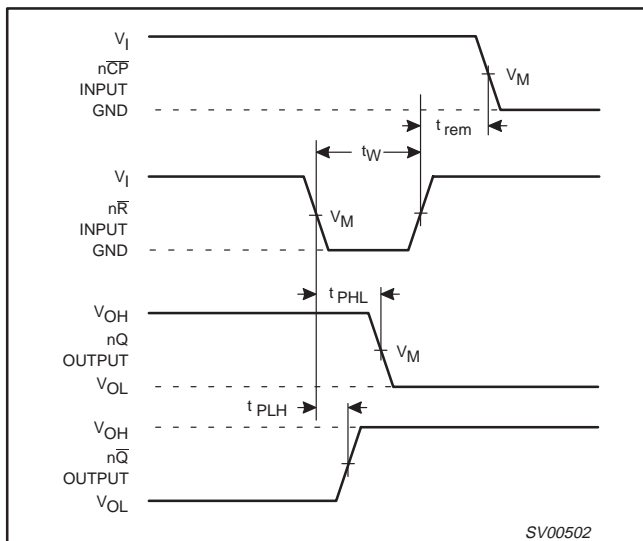
74LV107

## AC WAVEFORMS

$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$  and  $\leq 3.6\text{ V}$ ;  
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$  and  $\geq 4.5\text{ V}$ ;  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

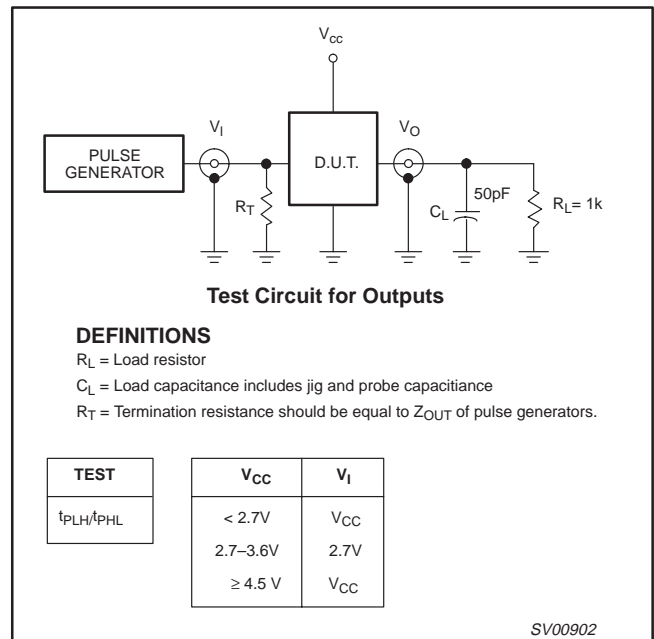


**Figure 1.** Clock ( $\overline{nCP}$ ) to output ( $nQ$ ,  $\overline{nQ}$ ) propagation delays, the clock pulse width, the J and K to  $\overline{nCP}$  set-up and hold times and the maximum clock pulse frequency.



**Figure 2.** Reset ( $\overline{nR}$ ) input to output ( $nQ$ ,  $\overline{nQ}$ ) propagation delays, the reset pulse width and the  $\overline{nR}$  to  $\overline{nCP}$  removal time.

## TEST CIRCUIT



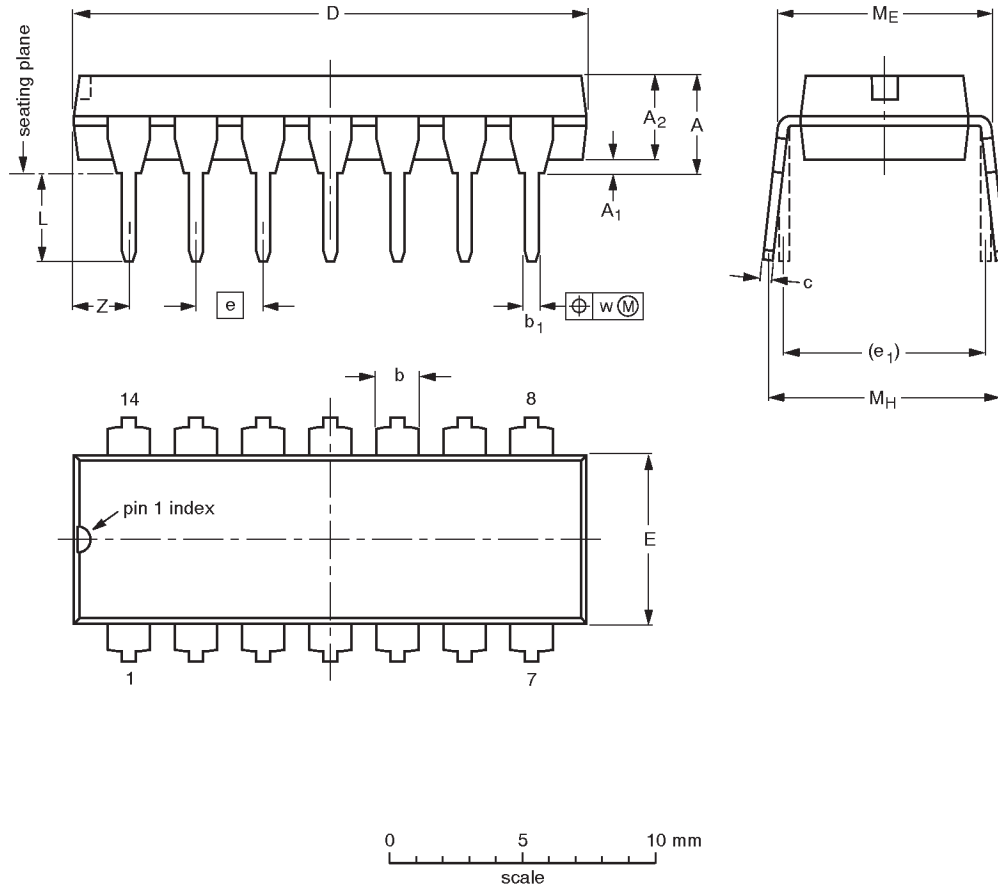
**Figure 3.** Load circuitry for switching times.

# Dual JK flip-flop with reset; negative-edge trigger

## 74LV107

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11

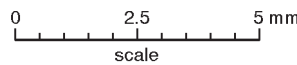
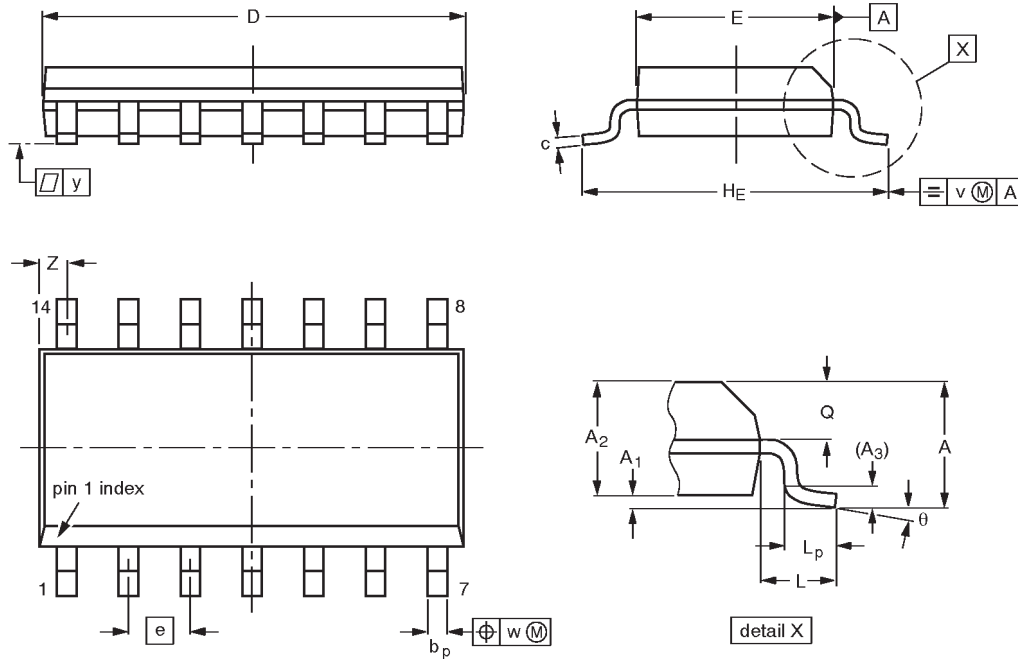


# Dual JK flip-flop with reset; negative-edge trigger

## 74LV107

**SO14: plastic small outline package; 14 leads; body width 3.9 mm**

**SOT108-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

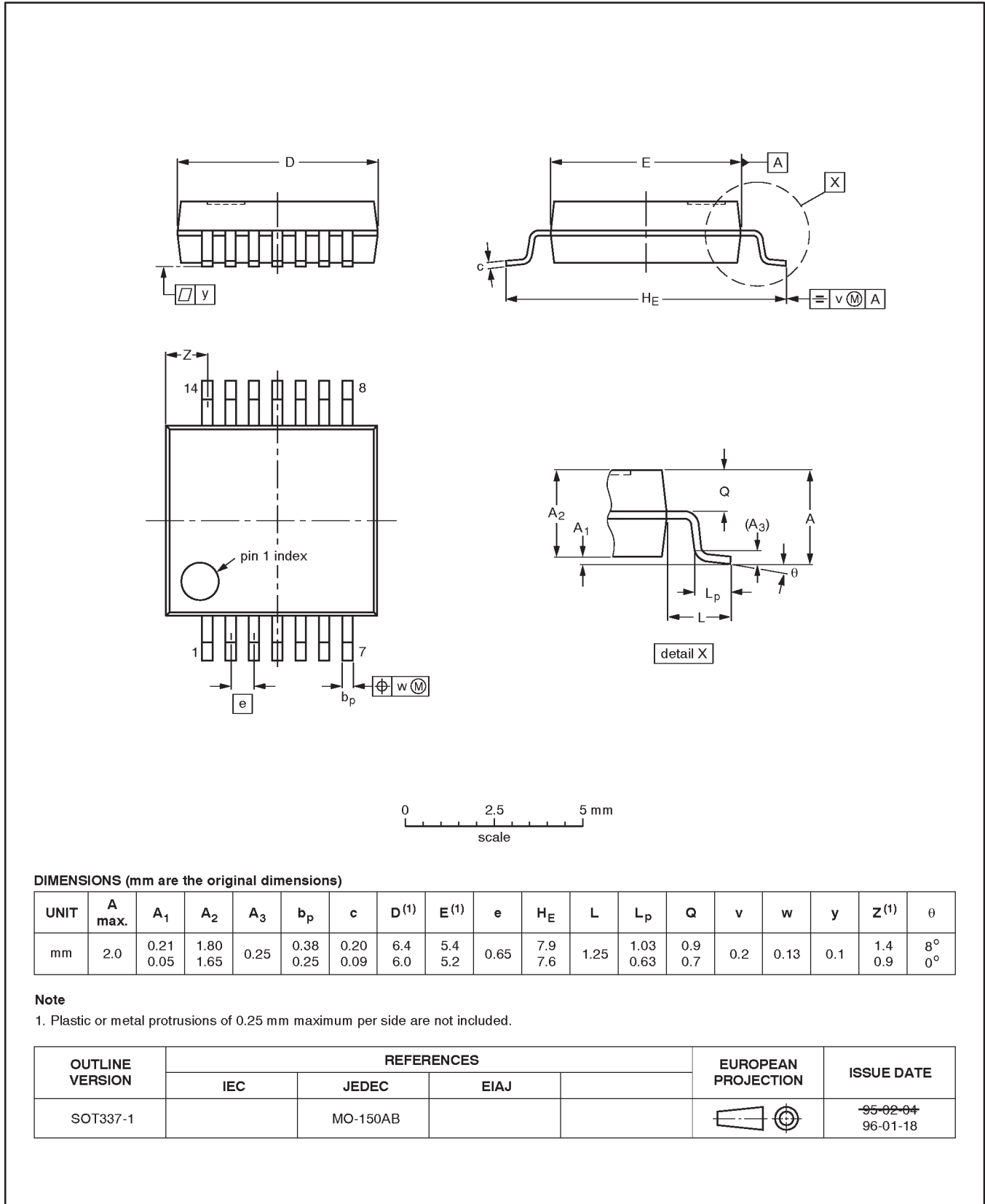
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-13 95-01-23

# Dual JK flip-flop with reset; negative-edge trigger

## 74LV107

**SSOP14:** plastic shrink small outline package; 14 leads; body width 5.3 mm

**SOT337-1**

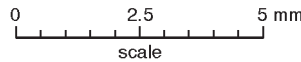
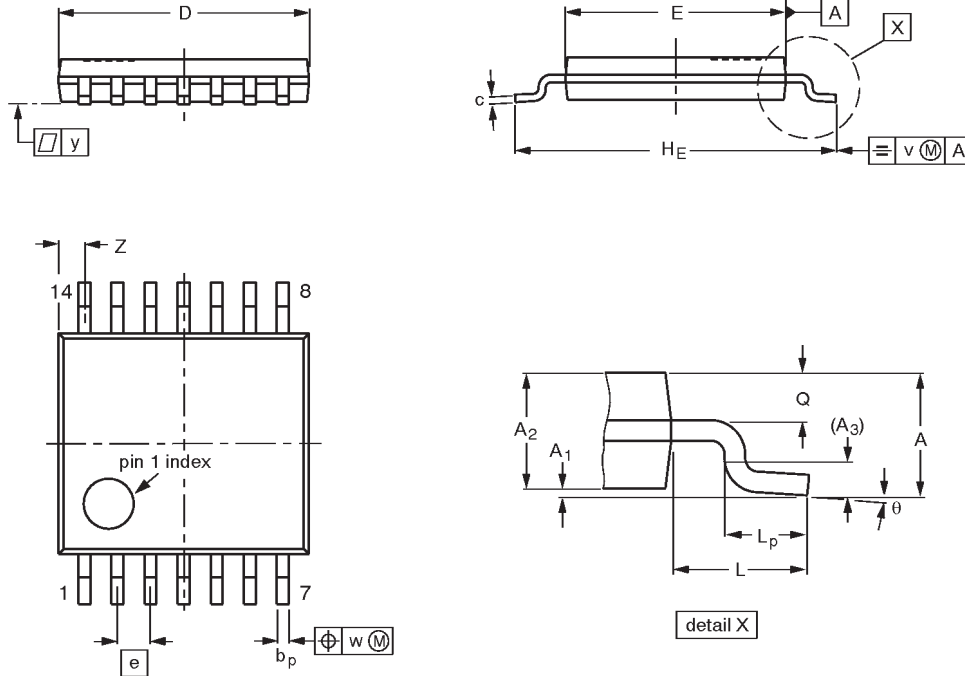


Dual JK flip-flop with reset; negative-edge trigger

74LV107

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-94-07-12- 95-04-04

## Dual JK flip-flop with reset; negative-edge trigger

74LV107

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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